Amendments to the Claims

The following listing of claims will replace all prior versions, and listings, of claims in the present application:

1. (currently amended) A method of forming interconnects in a semiconductor device by filling openings extending through a dielectric layer to an underlying conductive layer supported by a substrate, said method comprising the acts of:

forming a first dielectric layer over a base layer of a semiconductor device;

forming openings in said first dielectric layer so as to expose contact regions within said base layer;

positioning a conductive material in said openings formed in said first dielectric layer such that said conductive material is in electrical contact with said exposed contact regions;

forming a second dielectric layer over said first dielectric layer and said conductive material;

forming openings extending through said second dielectric layer such that said openings extend from an upper surface of said dielectric layer to said underlying conductive material in said openings formed in said first dielectric layer;

forming a malleable conductive layer over said upper surface of said dielectric layer and within said openings extending through said second dielectric layer, wherein a thickness of said malleable conductive layer is substantially less than a thickness of said dielectric layer such that said malleable conductive layer lines said opening and an uppermost surface of said malleable conductive layer defines an unfilled void extending upwardly from said uppermost surface of said malleable conductive layer within said opening; and

moving a portion of said malleable conductive layer formed over said upper surface of said dielectric layer into said unfilled void by polishing said malleable conductive layer so as to plug said opening.

2. (Original) A method of forming interconnects as claimed in claim 1 wherein said openings extending through said second dielectric layer are substantially vertically aligned with associated ones of said openings in said first dielectric layer.

3. (canceled)

4. (currently amended) A method of forming interconnects as claimed in claim 1 [~~3~~] wherein said malleable conductive layer is polished using a slurry mixture comprised of a slurry, said slurry comprising an alumina abrasive and a neutral to slightly basic pH, wherein said slurry is free of an oxidizer.

5. (Original) A method of forming interconnects as claimed in claim 4 wherein said slurry mixture further comprises a diluting solution mixed ten parts of said diluting solution to one part of said slurry.

6. (Original) A method of forming interconnects as claimed in claim 1 wherein said malleable conductive layer comprises a silver-based conductive material.

7. (Original) A method of forming interconnects as claimed in claim 1 wherein said conductive material positioned in said openings formed in said first dielectric layer comprises a tungsten-based conductive material.

8. (Original) A method of forming interconnects as claimed in claim 1 wherein said first dielectric layer comprises a silicon nitride layer.

9. (Original) A method of forming interconnects as claimed in claim 1 wherein said second dielectric layer comprises a silicon nitride layer.

10. (Original) A method of forming interconnects as claimed in claim 1 further comprising the acts of:

removing a portion of said malleable conductive material plugging said unfilled void;

depositing a chalcogenide in place of at least a portion of said removed malleable conductive material;

processing said semiconductor device so as to dope said deposited chalcogenide with material from said malleable conductive material plugging said unfilled void.

11. (Original) A method of forming interconnects as claimed in claim 10 wherein said portion of said malleable conductive material is removed by etching back said malleable conductive material.

12. (Original) A method of forming interconnects as claimed in claim 10 wherein said chalcogenide is deposited by forming a chalcogenide layer over said dielectric layer and said malleable conductive material plugging said unfilled void.

13. (Original) A method of forming interconnects as claimed in claim 12 wherein said chalcogenide is deposited by further polishing said device by removing portions of said chalcogenide layer not formed over said malleable conductive material plugging said unfilled void.

14. (Original) A method of forming interconnects as claimed in claim 10 wherein said doping process comprises a heating step, exposure to ultra violet radiation, or combinations thereof.

15. (Original) A method of forming interconnects as claimed in claim 10 wherein said doping process yields a solid solution comprising said chalcogenide and said malleable conductive material.

16. (Original) A method of forming interconnects as claimed in claim 10 wherein said chalcogenide comprises a combination of selenium and germanium.

17. (currently amended) A method of forming interconnects in a semiconductor device by filling openings extending through a dielectric layer to an underlying conductive layer supported by a substrate, said method comprising the acts of:

forming a dielectric layer over a base layer of a semiconductor device;

forming openings extending through said dielectric layer such that said openings extend from an upper surface of said dielectric layer to said underlying conductive material in said openings formed in said first dielectric layer;

forming a malleable conductive layer over said upper surface of said dielectric layer and within said openings extending through said dielectric layer, wherein a thickness of said malleable conductive layer is substantially less than a thickness of said dielectric layer such that said malleable conductive layer lines said opening and an uppermost surface of said malleable conductive layer defines an unfilled void extending upwardly from said uppermost surface of said malleable conductive layer within said opening;

moving a portion of said malleable conductive layer formed over said upper surface of said dielectric layer into said unfilled void by polishing said malleable conductive layer so as to plug said opening;

removing a portion of said malleable conductive material plugging said unfilled void;

depositing a chalcogenide in place of at least a portion of said removed malleable conductive material;

processing said semiconductor device so as to dope said deposited chalcogenide with material from said malleable conductive material plugging said unfilled void.

18. (Original) A method of forming interconnects as claimed in claim 17 wherein said portion of said malleable conductive material is removed by etching back said malleable conductive material.

19. (Original) A method of forming interconnects as claimed in claim 17 wherein said chalcogenide is deposited by forming a chalcogenide layer over said dielectric layer and said malleable conductive material plugging said unfilled void.

20. (Original) A method of forming interconnects as claimed in claim 17 wherein said chalcogenide is deposited by further polishing said device by removing portions of said chalcogenide layer not formed over said malleable conductive material plugging said unfilled void.

21. (Original) A method of forming interconnects as claimed in claim 17 wherein said doping process comprises a heating step, exposure to ultra violet radiation, or combinations thereof.

22. (Original) A method of forming interconnects as claimed in claim 17 wherein said doping process yields a solid solution comprising said chalcogenide and said malleable conductive material.

23. (Original) A method of forming interconnects as claimed in claim 17 wherein said chalcogenide comprises a combination of selenium and germanium.